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VLSI Floorplanning / Simulated Annealing. This applet illustrates the application of Simulated Annealing to VLSI Floorplanning. Simulated Annealing is a general approach to optimization in which small transformations called moves are randomly applied to a configuration (in our case, floorplanning). Moves that decrease the cost of the configuration are always accepted, while moves that increase the cost function are accepted probabilistically under the control of a temperature parameter.

VLSI Floorplanning / Simulated Annealing - John A. Nestor

This new method is called simulated annealing. It's a very famous general optimization method. You can optimize lots of different things with it. It is, however, widely used in VLSI CAD. It



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was invented at IBM in the early 1980s by Kirkpatrick, Gelatt, and Vecchi, from this very famous paper from Science Magazine.

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Simulated annealing is a probabilistic technique for approximating the global

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optimum of a given function. Specifically, it is a metaheuristic to approximate global optimization in a large search space for an optimization problem. It is often used when the search space is discrete. For problems where finding an approximate global optimum is more important than finding a precise local optimum in a fixed amount of time, simulated annealing may be preferable to exact algorithms such as gradient des

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Aaquil Bunglowala and Manisha Jain.

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